Description of the IPHT sub-µm cross-type JJ technology with ground plane

Process Name: CJ2

Version Number: 1.1

Version Date: 21.11.2023

1. General remarks

- Fabrication on 100 mm (4 inch) Si wafers, 500 µm thickness with 600 nm thermal SiO_2 surface,
- Typical size of a single chip is 2.5 mm x 2.5 mm, including dicing channels (please refer to 4.); other chip sizes on request,
- standard cross-type Josephson junction (JJ) process with added ground plane underneath,
- standard critical current density of 1.7 kA/cm^2; other current densities on request,
- in-situ deposited Nb/Al-AlOx/Nb trilayer for the JJs,
- Nb as material for wiring layers; AuPd for the resistors (shunt, bias) and bond pads,
- overall grid size for design is 0.1 µm,
- layer-to-layer overlap (edge-to-edge distance) is 0.5 µm; parallel edges of different layers on identical positions are forbidden,
- designs should be provided in gds2 format.

2. Layer Specification

GDS2 layer No.	Layer name	Material	Thickness [nm]	Description	Polarity
17	WIR1	Nb	200	Ground plane deposition	draw remaining metal parts
11	MOAT			Moats in WIR1	WIR1 minus MOAT
12	ISO1	SiO_2	250	Isolation above Ground plane	draw openings in ISO1
1	TRI	Nb/Al/Nb	100/14/60	Trilayer deposition, (TRI-top, TRI-barrier, TRI-base)	draw remaining metal parts
2	WIR2	Nb	250	Deposition of WIR2, not covered TRI will be etched exception Tri-base	draw remaining metal parts
3	VIA			Contact between TRI/ WIR1 and WIR2, and openings for CUT	draw openings in VIA
4	CUT			Removal of TRI-base	draw to be removed CUT
5	ISO2	SiO_2	300	Isolation below WIR3 with contact holes to WIR2, TRI-base or WIR1	draw openings in ISO2
6	WIR3	Nb	350	Deposition of WIR3	draw remaining metal parts
7	RES	AuPd	80	deposition resistor	draw remaining metal parts
8	ISO3	SiO_2	300	Deposition of cover for mechanical protection	draw openings in ISO3

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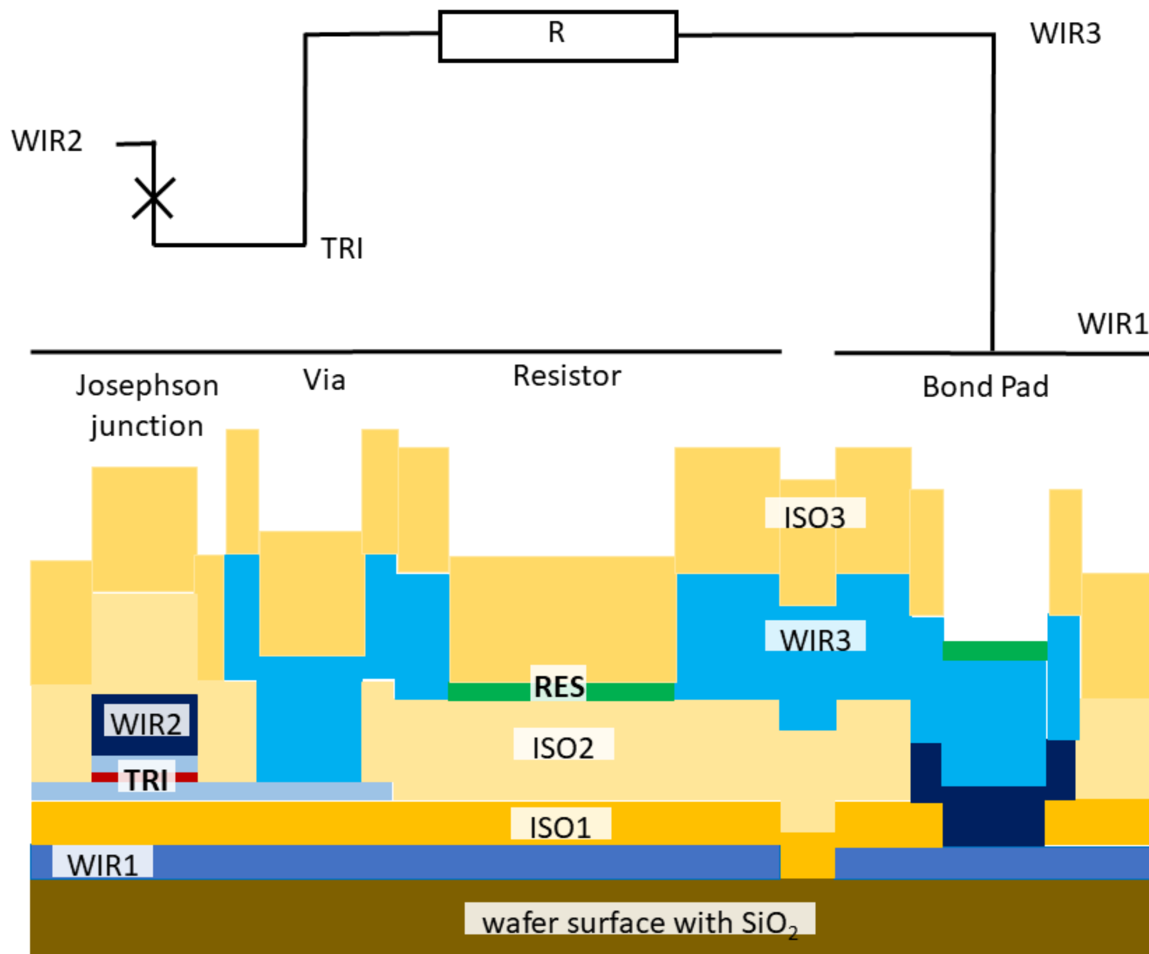
- drawing in corresponding layers in design file means that:
    - drawing will result in remaining structures in metal layers, except for layer WIR1 – here openings in Nb layer/ moats will be drawn,
    - drawing will result in openings in VIA, CUT, ISO1, ISO2, ISO3,
- auxiliary layer 13 is used for text and labels on the chips, which will be converted as additional openings in ISO2,
- During chip placement into the wafer frame a position label text is added as additional openings in ISO3.



3. Design Rules

3.1 Stripline inductance

- inductances were measured in parallel field interferometers with micro-strips of two different length and width,
- up to now, only devices in the conventional cross-type process without ground plane have been realized, consisting of TRI base electrode (60 nm) / WIR3 (350 nm),

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- the isolations ISO2 and ISO3 in the ground plane process have a thickness of 300 nm, which is the same as for isolation between TRI base and wiring layer in the conventional cross-type process, so the values listed below can be seen as first assumptions of stripline inductances within this process,
- more precise values will be updated as soon as samples are fabricated and measured.

Layer	Stripline width in µm	Square inductance in pH/square
TRI-base/ISO2/WIR3	4 / 2	0.31
TRI-base/ISO2/WIR3	6 / 3	0.43
TRI-base/ISO2/WIR3	50 / 3	0.56

3.2. Layer description

A. WIR1 Nb Ground plane

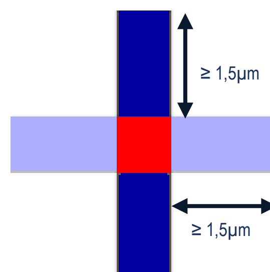
- minimum openings (moats) are 2.5 µm with a 2.5 µm spacing. The ground plane is recommended for digital circuits. In analogue circuits this WIR1 layer can be used as additional wiring layer.

B. ISO1 Isolation

- minimum openings are 4 µm x 4 µm,
- connection WIR3 to ground plane is only possible via WIR2. This will e.g. result in stacked vias for connection between WIR3 and ground plane.

C. TRI Josephson Junction definition

- junction definition achieved by overlap of two perpendicular strips of TRI and WIR2, junction size is therefore due to the width of the two strips,
- every overlap between TRI and WIR2 will result in Josephson junctions,
- Josephson junctions with square shape are recommended,
- minimal protrusion of the strips is 1.5 µm to each side next to the junction,



- design value of the junction dimensions have to be resized by additional 100 nm to each edge due to shrinkage in the process (that means, for a 1 µm x 1 µm junction on the chip both strips have to be 1.2 µm wide in design),
- minimum TRI and WIR2 pattern width are 800 nm and therefore real minimum JJ size is 600 nm x 600 nm,
- only TRI areas with WIR2 on top remain the full trilayer stack, for all other TRI areas remain 60 nm niobium which can be used as wiring layer with minimum feature size and minimum line space of 2.5 µm.

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- For a required process step, all TRI structures must be electrically connected to a common wafer terminal. Also, the total overlap area of WIR2 structures over TRI must be >= the larger of 9 μm^2 or 5 times the area of all WIR2 structure embedded JJs. VIA and CUT structures are required to remove unwanted connections later by an etching process. Usually, the TRI connection to the wafer can be done by a chip frame loop in TRI.

D. WIR2 wiring layer
- Please note: the WIR2 layer is mainly to build and connect the Josephson junction (see 3.2 C.), but it can carefully be used as wiring layer with minimum feature size and minimum line space of 2.5 µm.

E. VIA Electrical contacts between layers and window for CUT
- the minimal contact size is 4 µm x 4 µm,
- contact size in Layer VIA determines minimum via size.

F. Layer CUT
- cut is only possible for the remaining 60 nm niobium of the TRI layer (see 3.2 C.),
- cut length have to be longer than 2 µm.

G. WIR3 wiring layer
- minimum feature size and minimum line space is 2 µm,
- The nominal maximum current for a 2 µm wide WIR3 wire is 1 mA. If higher values are requested, please get in touch with the foundry representatives.

H. RES Resistor for shunt and bias
- The design value of the sheet resistance at 4.2 K is 3 Ω/□,
- Process shrinkage is about 0.5 µm to all edges; the electrically resistor length is defined by the distance of two WIR3 contact terminals; minimum overlap of the resistor terminal to Layer WIR3 is 3 µm, recommended minimum resistor width is 3 µm,
- Crossing edges of RES material to underlying structures is forbidden (except WIR3 for contacting RES),
- The bond pads can be covered by RES to improve the bonding adhesion.

I. ISO3 Cover
- whole chip area excluding the bonding pads is typically covered by layer ISO3,
- Recommendation is to use the ISO3 cover layer for text and labels on the chips and chip positions.

4. Effective chip area

- there is a dicing channel to each side of the chip with a width of 100 µm,
- The usable chip area is therefore 2.4 mm x 2.4 mm,
- larger chip sizes are possible on request.

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